Toward Industrial-Scale Fabrication of Nanowire-Based Devices

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Although optical lithography is suited for producing intricate architectures, its combination with "bottom-up" approaches becomes a very challenging issue. The challenge is to electrically address the coordinates of millions of nanoparticles (e.g., nanowires) on a given surface. Here, we describe a method that controls the registries of *horizontally* grown nanowires (NWs) and advances the current state-of-the-art NW device assembly technology. In this architecture, NWs are grown where the nanodevices will later be fabricated on. There is no need to transfer NWs to a different surface or align them. With the use of only three photolithographic steps, this technique allows industrial-scale production of nanodevices. First, an α-plane sapphire surface is patterned with gold nanodroplets. Next, small-diameter zinc oxide NWs are grown selectively on the predefined gold sites. Growth direction of the NW is controlled using the anisotropic crystal match between zinc oxide and the underlying substrate. Subsequently, metal electrodes are deposited on NWs at once and in a parallel fashion. To demonstrate the capabilities of this method, large numbers of top-gated zinc oxide NW field-effect transistors are prepared using optical lithography. This fabrication method opens the path to a new generation of nonconventional nanodevices and nanosensors and could impact nanotechnology industries.

Introduction

Since the emergence of nanostructures as technologically relevant materials, "bottom-up" fabrication strategies and directed assembly methods have become increasingly attractive. Due to their potential for new generations of electronic devices, the need for their development has been noted in the International Technology Roadmap for Semiconductors.[1] In the current state-of-the-art "bottom-up" assembly of nanowire (NW)-based devices, multistep treatments and removal and alignment of NWs are necessary steps that often impose limitation on nanofabrication at technologically relevant scales. In aligning NWs, several strategies aiming at controlling their hierarchy have been developed such as electric field assisted orientation[2] and alignment with fluid flow in microchannels.[3] More recent advances have been the confinement and alignment of NWs using the Langmuir−Blodgett technique,[4] assembly of densely packed elongated metal NWs using a pattern transfer process,[5] and large-area blown bubble films of aligned NWs.[6]

Herein, we demonstrate a fabrication technique that combines a "bottom-up" chemical approach with conventional photolithography. It exceeds the current state-of-the-art assembly of NW-based devices and results in three important advances to the field. The first is defining the starting coordinates of horizontally grown NWs. Since the growth direction of NWs is known, the end point coordinates of NWs become known as well. Therefore, the devices would be exactly fabricated where horizontal NWs are residing. Second, this method allows control over the number of NWs in each device. This is because each NW is grown from a gold nanodroplet, thus controlling this number results in control over the number density of NWs. Third, this is a scalable technique capable of industrial-scale applications in its current status. To demonstrate the potentials of this method, we fabricated NW field-effect transistor (FET) devices with one, two, or several NWs. Also using this platform, an interesting distinction between electrical properties of individual and ensembles of NWs was found.

Zinc oxide, a sensor, piezoelectric, UV light emitter, and transparent semiconductor in the visible spectrum, is a technologically important material.[7−9] In the method reported here, we use an individual gold nanodroplet to horizontally grow a ZnO NW on α-plane $(11\bar{2}0)$ sapphire. Horizontal NWs are a new class of NWs which can be grown in a tube furnace at ambient pressure via a physical phase transport process (Experimental Section). The anisotropic growth of a NW starts at the initial nanodroplet location and continues along the $[1\bar{1}00]_{sap}$ of sapphire as the nanodroplet moves on the surface.[10] In this direction, the ZnO (*c*-plane) and sapphire (α-plane) have a close lattice match along their "*a*" and "*c*" axes, respectively.[11] Intentional anisotropic crystal growth

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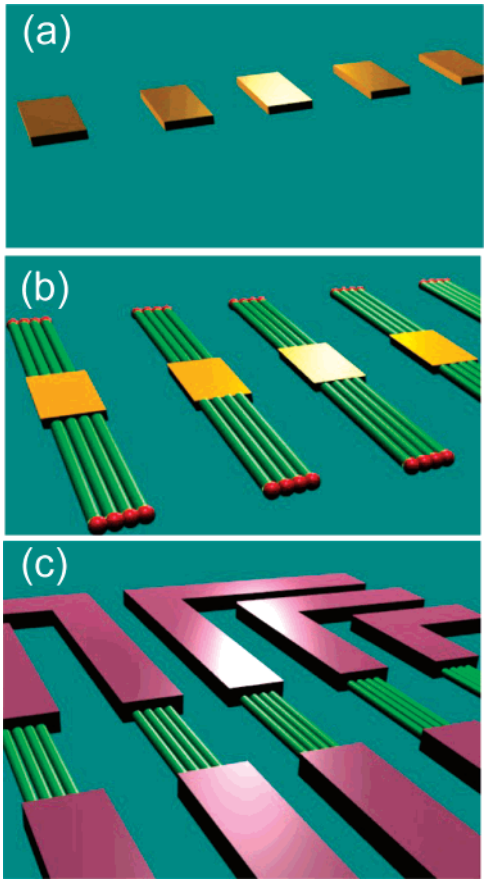

Figure 1. Schematic of the photolithography process for scalable fabrication of nanowire devices. (a) Gold pads and fiducial marks are deposited on the surface. (b) NWs are grown selectively from the two sides of the gold pads. (c) Metal electrodes and bonding pads are placed exactly on NWs by alignment of fiducial marks.

was first illustrated by Chen and co-workers in growth of one-dimensional rare-earth silicides on Si (001).[12,13] The lack of control over the location and orientation of the formed NWs remained the main shortcoming of such techniques. In this work, the distinction is the localized and confined growth of ZnO NWs using gold nanodroplets as "mobile crystal growers".

Our strategy to integrate NWs into nanodevices included a two-step photolithography process, which is schematically described in Figure 1a−c. First, small gold pads and fiducial (global) marks are placed on a sapphire surface (Figure 1a). ZnO NWs are then epitaxially grown at the two sides of each pad in opposite directions (Figure 1b). In the second photolithography step, patterns of metal electrodes are placed on NWs (Figure 1c). A third step of photolithography, which places the top gate electrode pattern on the NWs, completes the fabrication of FETs. Most significantly, this method is a parallel nanofabrication process. It does not require serial device fabrication using high-resolution lithography methods such as electron beam lithography (EBL). These steps are described in further detail in the following sections.

Experimental Section

ZnO NWs were grown via a phase transport process using gold nanodroplets as nucleation sites. We used the growth method developed for growth of standing NWs[14−16] and modified it for promoting the horizontal growth of NWs.[10] For gold nanodroplets less than 25 nm in size, previously, we observed in-plane and oriented growth of small-diameter NWs on α-plane sapphire. Briefly, ZnO/graphite mixture (0.15 g, 1:1 mass ratio) was loaded on a Si substrate and positioned at the center of an inner tube (13 cm length, 1.9 cm i.d.). Subsequently, this tube containing a sapphire substrate was inserted into a tube furnace such that the mixed powder was placed at the center of an outer tube (80 cm length, 4.9 cm i.d.). The tube furnace temperature was set at 900 °C (with a ramp rate of 110 °C/min) for 10 min under 0.6 SLPM (standard liters per minute) flow of 99.99% Ar gas.

For patterning the sapphire surface with gold, 8 mm × 8 mm α-plane sapphire pieces were washed with small cotton swabs and deionized water (DI water) and then nitrogen (99.99%) dried. Following photolithography protocols, samples were coated with photoresist. Patterns of 1 μm × 5 μm pads along with fiducial marks were created on the photoresist. Thin gold films, 1−3 nm, were deposited on photoresist using a thermal evaporator. Photoresist lift-off was carried out in acetone for at least 45 min (Supporting Information). After 3 min of ozone cleaning, the washed and dried substrate was transferred to the end of the small quartz tube and NWs were grown according to the procedure described earlier.

Results and Discussion

In the first step of photolithography, 1 μm × 5 μm gold pads (and fiducial marks) were deposited such that their long sides were parallel to the $[1\bar{1}00]_{sap}$ direction of the sapphire wafer (Figure 2a). A closer view of the positioning of the gold pads relative to the NW growth direction is shown in Figure 2b. An atomic force microscopy (AFM) line profile of a gold pad is illustrated in Figure 2c which shows an average height value of 2.5 nm for gold pad thickness. Typically, a gold thickness ranging from 2 to 8 nm is suitable for the horizontal NW growth. After the growth, nanodroplets residing at the two short sides of each gold pad produced densely packed horizontal ZnO NWs. An AFM image of this selective and oriented growth is shown in Figure 3a. The AFM height profile of these NWs in Figure 3b shows that NW diameter ranges from 8 to 13 nm. Typically, gold pads with 3 (±1) nm thickness resulted in NWs with an average thickness of 11 (±3) nm, and the NW density per pad width was found to be 10 NWs/μm. This number can be further reduced by decreasing the number of gold nanodroplets or by increasing the resolution of the optical lithography. Horizontal NWs are epitaxially grown on sapphire and are not readily removed from the surface. On the basis of SEM and AFM size measurements, width to height ratio of NWs was typically found to be close to one; therefore a semicircular profile was assumed for horizontal NWs. An SEM image of another group of NWs is shown in Figure 3c. This figure also shows that standing NWs are

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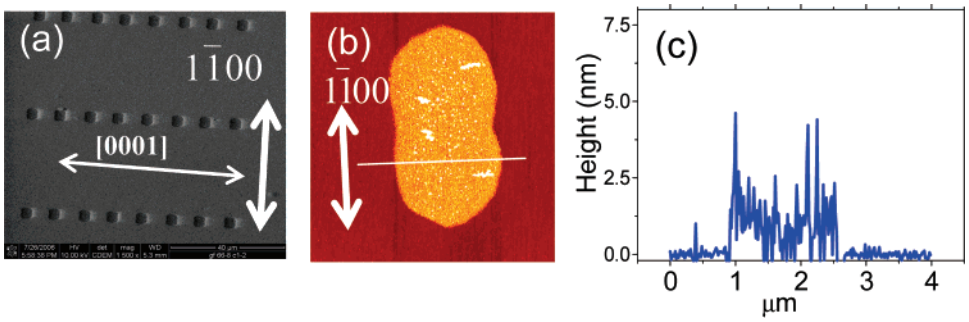

Figure 2. SEM and AFM images of gold pads and their orientation relative to NW growth direction. (a) SEM image of gold pads after photoresist lift-off. Pads are placed such that their smaller edges are perpendicular to the growth direction of NWs (shown with white arrows). (b and c) AFM image of a gold pad and its AFM line profile.

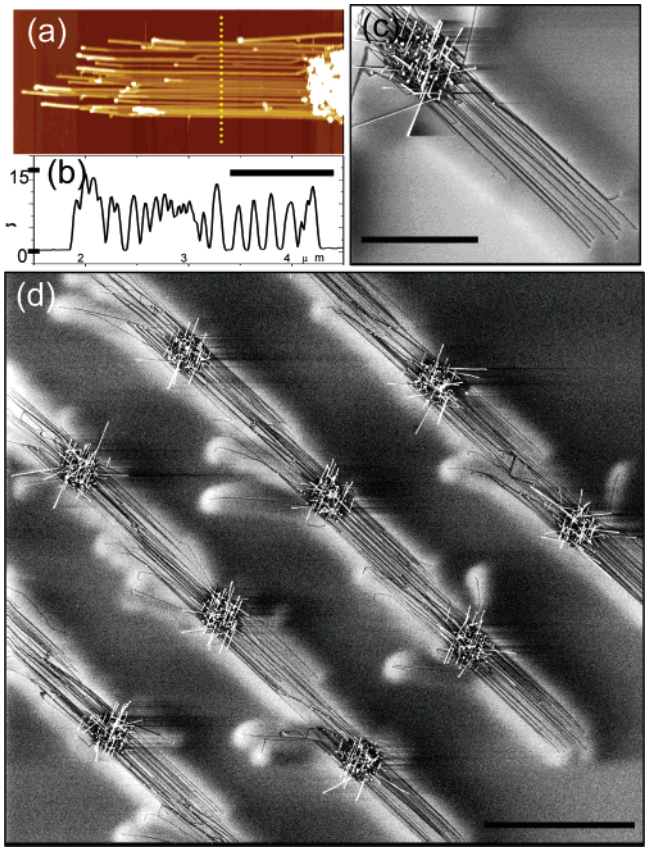

Figure 3. AFM and SEM images of site-selective growth of horizontal NWs. (a) AFM image of a group of about 23 NWs grown from a gold pad. (b) AFM height profile along the dotted line of these NWs shows the NW diameter ranges from 8 to 13 nm. Scale bar, 1 μm. (c) SEM image of a group of 12 NWs. Scale bar, 4 μm. (d) Directed growth of NWs at predefined locations on a large scale. Scale bar, 10 μm.

grown during the process.[16] Figure 3d is an example of site-selective, directed, and scalable growth of NWs seeded directly by gold pads on α-sapphire substrate.

In the second step of photolithography, using the fiducial marks already on the surface (from step 1), integration of NWs and metal electrodes into devices was carried out by aligning these marks with the complementary ones on the photolithography mask. Metal electrode patterns were placed on NWs across the whole 8 mm × 8 mm substrate with a good precision that was limited to the resolution of the mask aligner. Figure 4a shows this overlap where the gold pads are seen as dark spots and the NW growth direction is shown with a red arrow. Alignment of NWs and electrodes was performed such that the left metal contact resided at the beginning of NWs. Depending on the number of grown NWs from a given gold pad, a nanodevice was comprised of single or multiple NWs. Examples of devices with a few NWs are shown in Figure 4b−d, and more examples are presented in the Supporting Information (Figure S2). Devices containing double and single NW with multiple metal electrodes are shown in Figure 5a−d (and Supporting Information, Figure S3). In the developed technique, we were able to achieve parallel fabrication of *nanodevices* using a photolithography process with 1 μm feature resolution. This is in contrast to the current state-of-the-art NW device fabrication in which registries of NWs are not known and single NW devices are typically fabricated randomly by EBL in a serial fashion.[17] As mentioned earlier, by increasing the resolution of the optical lithography, a better control over the number of NWs is expected. Considering the current advances in semiconductor industry for feature miniaturization, the present technique is well suited for producing a new generation of nanodevices with densities comparable to the current technology.

Electrical transport measurements presented here were carried out on three different batches of chips. In a single fabrication process, more than 600 nanodevices can be prepared composed of both single and multi-NW devices (Supporting Information, Figure S2). More than 20 nanodevices from the aforementioned batches were tested repeatedly over the course of 3 months; during this period none showed any evidence of degradation or aging. The NW FET devices were fabricated by first depositing a 60 nm thick silicon oxide layer on the entire substrate using a plasma-enhanced chemical vapor deposition technique. Subsequently, gate electrodes were placed on their exact locations via a third step of photolithography. In the devices studied, the NWs as well as part of the source-drain electrodes were covered by the gate electrode (Supporting Information, Figure S2). All reported electrical transport measurements of single NW or groups of NWs were measured at room temperature and ambient pressure. In the studied NW devices, the number of NWs ranged from 1 to 8.

Typical current versus source-drain voltage ($I_{DS}-V_{DS}$) scans are shown in Figure 6, parts a and b, for a multi-NW and a two-NW device, respectively. At a positive (negative) gate bias, the I_{DS} increases (decreases) markedly; hence the

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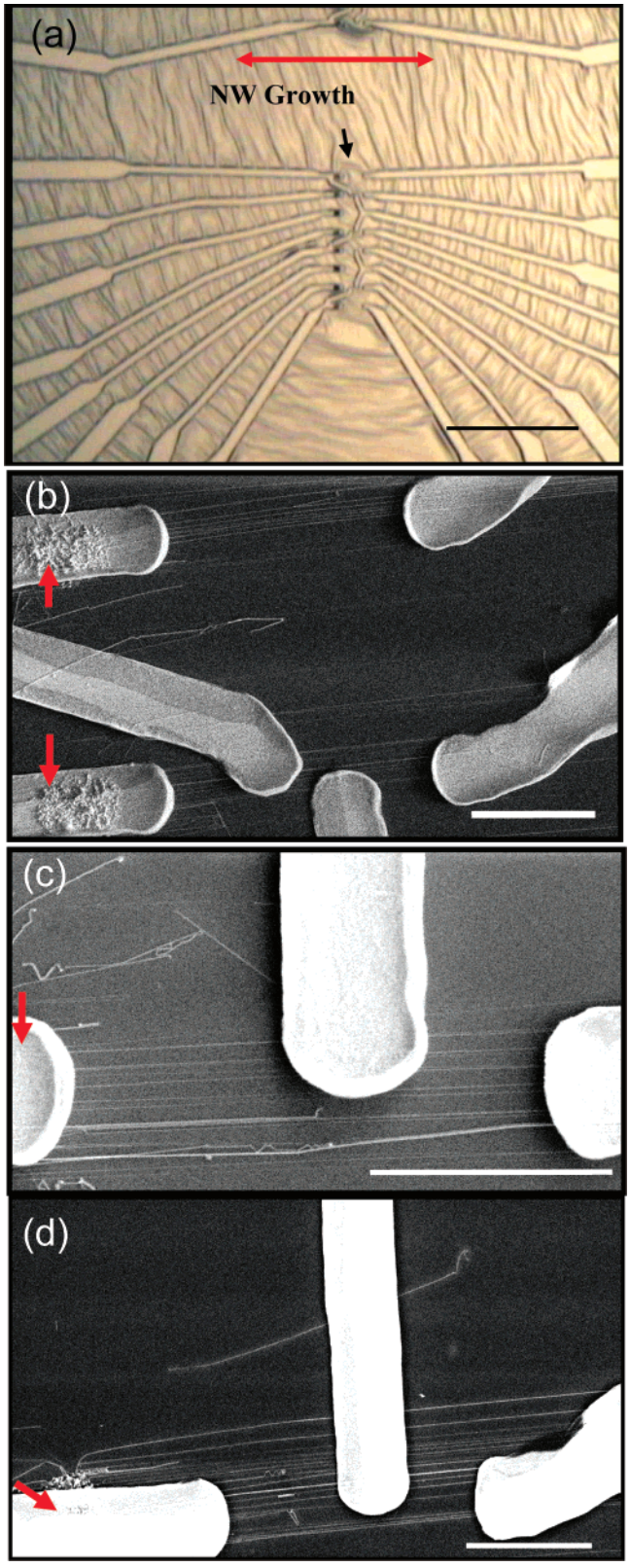

Figure 4. Integrating NWs and metal electrodes using optical lithography. (a) An optical image illustrates integration of metal electrodes with NWs. The dark spots are the original gold pads which contain the NWs on both their sides (shown with the black arrow). The red arrow shows the growth direction of NWs relative to the metal electrodes. The coordinates of gold pads are fixed and known relative to the fiducial marks. Scale bar is 50 μm. (b−d) SEM images of metal electrodes connected to a group of NWs. The scale bars in (b−d) are 5 μm.

channel is n-type.[18] The gate modulation efficiency was further investigated by plotting $I_{DS}-V_G$ for a variety of

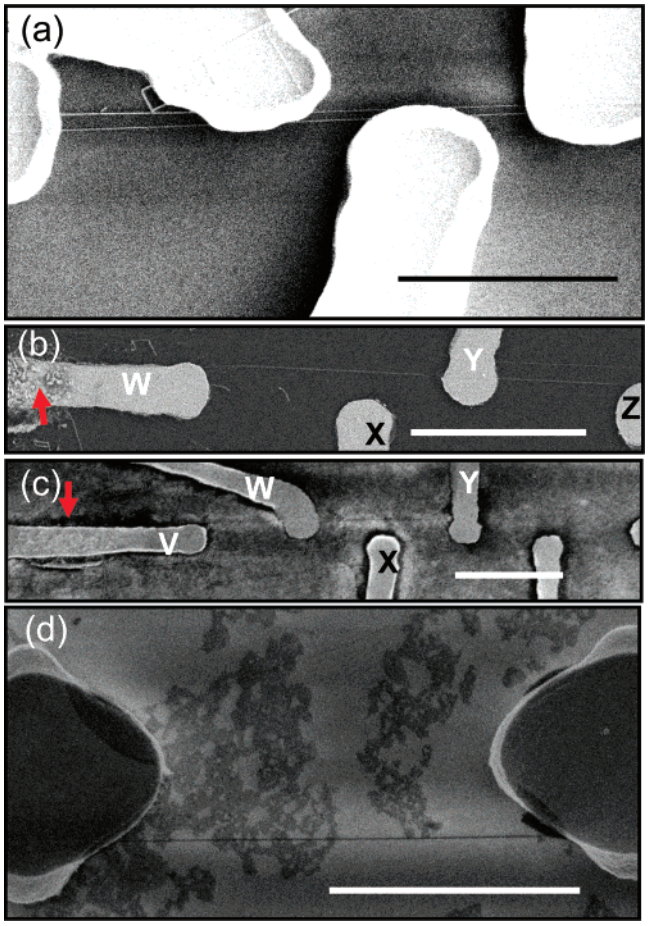

Figure 5. (a) Device containing two NWs. (b−d) Single NW devices with two or more electrodes fabricated by only photolithography. The scale bars in (a−d), 5 μm.

source-drain voltages (Figure 6, parts c and d). For such devices the threshold voltage was found to be about −3 V, an indication of a "depletion mode" FET.[19] The field-effect mobilities for the multi-NW and two-NW devices were found to be ∼15 and 20 cm^2/Vs at V_{DS} of 1 V.[19,20] In calculating the mobility, the channel width was assumed to be the sum of the diameters of the NWs. Although the profile of NWs is closer to a semicircular shape, for estimating the field-effect mobilities, the NW profile was considered circular. The on/off current ratios of the devices were found to be about 10^5 at V_{DS} of 4 V. Devices with multiple NWs, due to their small diameters and larger surface areas, are expected to be suitable for sensing application as compared to thicker (e.g., 100 nm diameter) single NW devices.

In examining several single NW devices with diameters less than 20 nm, $I_{DS}-V_{DS}$ measurements showed both linear and rectifying behaviors (Supporting Information, Figure S4). Figure 6e shows the $I_{DS}-V_{DS}$ data collected at different gate biases for a NW with 14 (±1) nm diameter and 7.1 μm channel length. An increase in the I_{DS} upon increasing the gate bias voltage can be seen. This device compared to the

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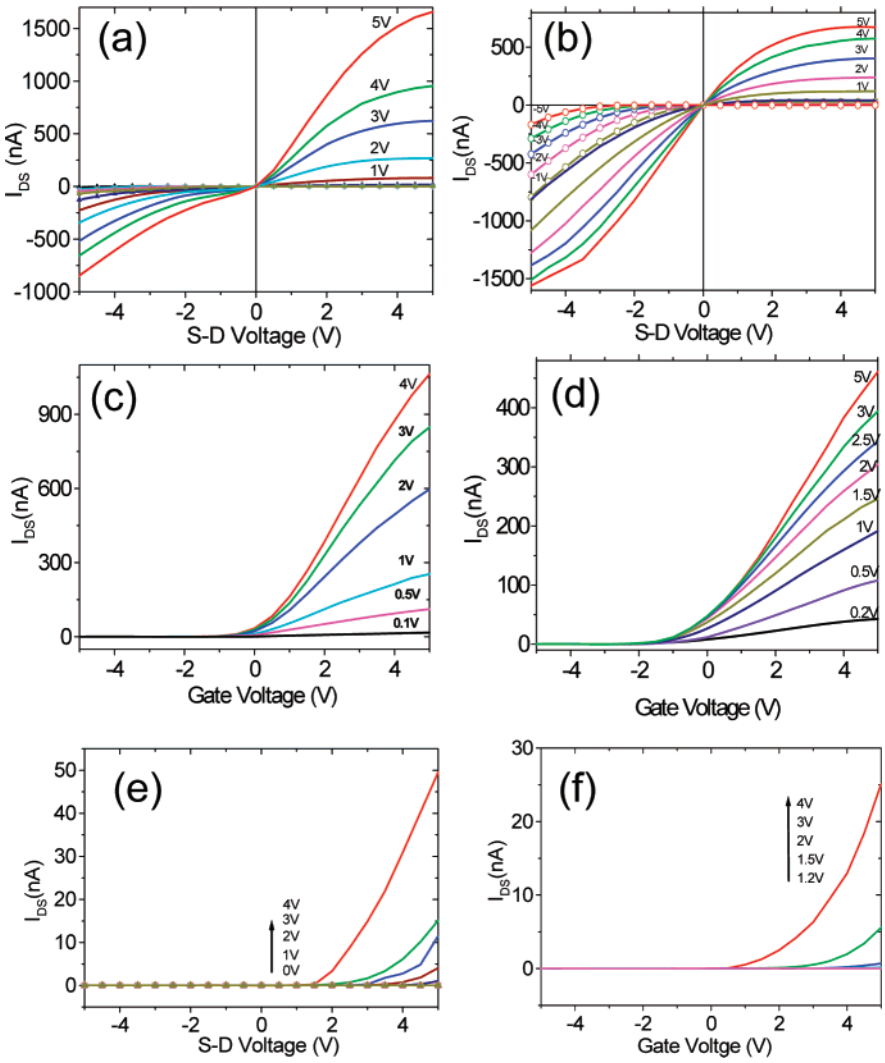

Figure 6. Current−voltage and transconductance measurements of NW devices. $I_{DS}-V_{DS}$ data for top-gated FET NW devices containing (a) eight NWs, with diameter distribution of 13 (±5) nm and channel length of 8.5 μm; (b) two NWs, 10 (±1) and 20 (±1) nm in diameter and a channel length of 6.3 μm. The scans were recorded at different gate voltages ranging from −5 to 5 V. In both devices, by increasing V_{DS}, I_{DS} linearly increased, followed by device saturation due to a drastic falloff in the charge carriers (electrons). When negative gate bias was applied (lines with symbols), channel conductivity gradually disappeared. At fixed V_{DS}, $I_{DS}-V_G$ scans were collected for (c) eight-NW device; (d) two-NW device. The absence of current saturation in this voltage range indicated low resistivity of the contacts. (e) $I_{DS}-V_{DS}$ scans for a single NW FET. The maximum drain current at V_{DS} of 5 V increased from 1 to about 50 nA within 0 to 4 V of V_G. (f) $I_{DS}-V_G$ curves show that the single NW device is not conducting at zero gate bias, which is different from multi-NW devices (c and d).

two-NW device (Figure 6b) shows a lower drain current, which could be due to Schottky contacts and smaller NW diameter. Figure 6f shows that the device remained off at zero gate bias indicating a very small conductive channel width. The threshold voltage was found to be about +1 V, an indication that the device was in the "enhancement mode". Among the tested devices, it was noticed that single NWs with diameters less than 15 nm tended to remain off under no gate bias. The observation of the two different modes in multiple and single NW devices is likely due to a decrease in the number of NWs and also their smaller diameter. In low-power applications, a device in the "enhancement mode" is more desirable over the "depletion mode" because there is no gate voltage necessary to turn the transistor off.[21] This is a remarkable property that can be used to tune the characteristics of a NW FET. The field-effect electron mobility measured for several single NW devices was found to be 4 (±2) cm^2/Vs with an on/off current ratio of at least $\sim 5 \times 10^4$. It is notable that the reported values above were obtained for device lengths ranging from 4 to 8 μm. NW surface engineering, i.e., overcoating the NW with a material with suitable band gap and lattice constant, is expected to decrease the number of electron scattering sites in the NW and therefore improve the electron mobility. In comparison to ZnO thin film transistors, ZnO NW devices show comparable electron carrier densities (10^{18} cm^{-3}) and field-effect mobilities but significantly lower threshold voltages.[21] In all of our fabricated devices, the threshold voltage (V_{th}) was found to be between 1 and −4 V originating from a gate dielectric thickness of about 60 nm. It is expected to have much lower V_{th} values and improved device behavior once a high-κ and structurally matched dielectric is used.[22] More comprehensive transport studies on single and group

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NWs are underway to further understand the electrical properties of this new class of nanomaterial.

A multitude of applications using this technique are possible. In the field of crystal growth, use of "mobile metal nanodroplets", such as gold, could be a new way for planar and localized growth of nanocrystals and their heterostructures. We have extended this approach to other (II−VI or III−V) semiconductor NWs that have anisotropic crystal mismatch with their underlying substrate. This technique in combination with other nanofabrication methods is expected to be used as a platform for building more complex architectures. Furthermore, it could be used as a template for growth and directed assembly of other important metallic or semiconductor nanostructures which cannot be prepared otherwise. This method, due to its scalability and ease of device fabrication, goes beyond the current state-of-the-art assembly of NW-based devices. It is believed to be an attractive approach for mass fabrication of NW-based transistors and sensors and is expected to impact nanotechnology in fabrication of nonconventional nanodevices.

Conclusion

A nanodevice fabrication method was described which is based on the combination of a "bottom-up" chemical method and conventional optical lithography. In comparison to other available techniques this method requires a minimum number of fabrication steps. The chemical method provides the horizontal growth of NWs from individual gold nanodroplets, and their alignment is dictated by lattice match with the underlying substrate. Locations of NWs, with a submicrometer precision, are controlled by the position of gold patterns made by photolithography. NWs are grown where the devices will be fabricated, and there is no need to transfer NWs to a different substrate. This approach in its current state seems to be a promising methodology for parallel nanodevice fabrication at technologically relevant scales.

Supporting Information Available: Additional experimental details, Figures S1−S4 (PDF). This material is available free of charge via the Internet at http://pubs.acs.org.

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